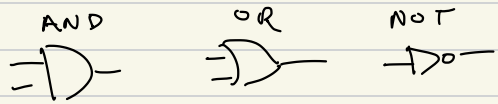
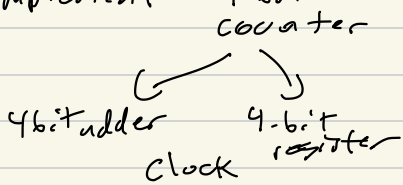
CS 631-01 Digital Design 2 2026-04-07

Today:
sequential Logic

Combinational Logic
sum-of-products



Implement: 4 bit counter

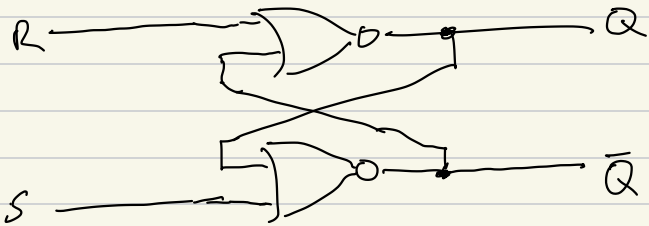


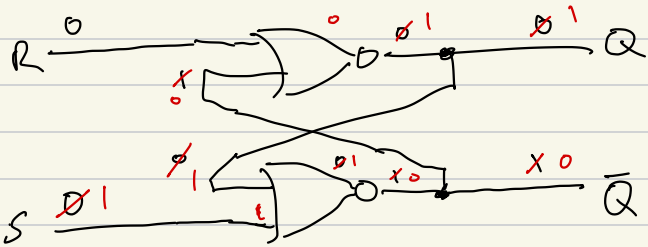
SR Latch

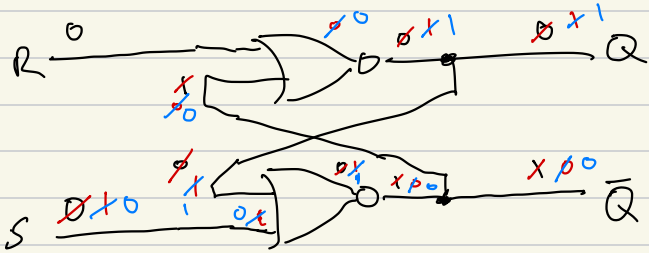
sub goal -> N-bit register

SR Latch
↓
Clock
↓
D Latch
↓
Multiplexor
↓
D Flip Flop
↓
D Flip Flop CLR EN
↓
1-bit Register

SR Latch Set Reset Static RAM

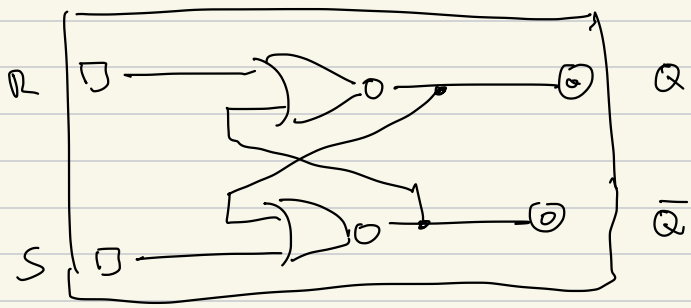




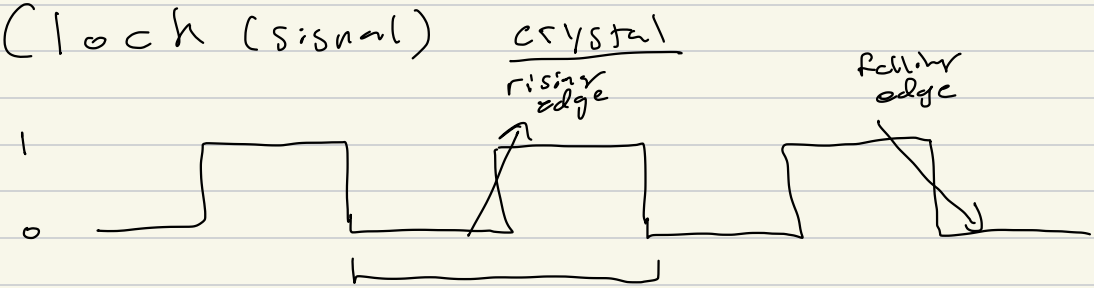


R	S	Q	$\bar{Q}$
0	0	0	1
0	1	1	0
0	0	1	0
1	0	0	1
0	0	0	1
1	1	X	X

SR Latch

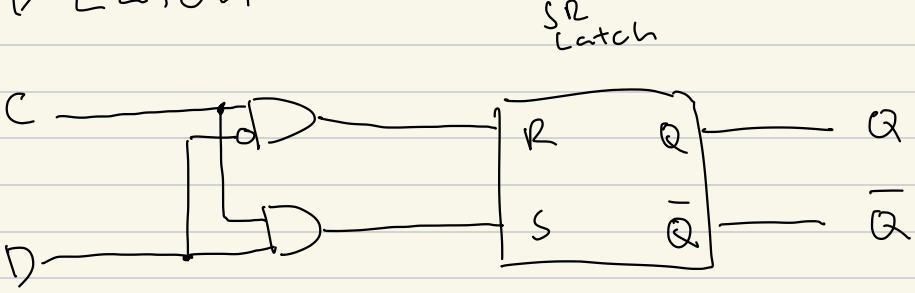


Clock (signal)



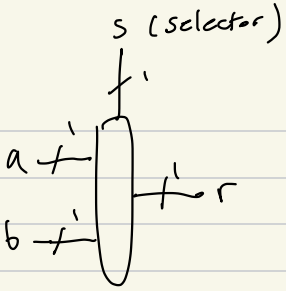
10 Hz
100 Hz
1 GHz

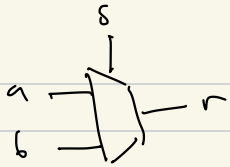
D Latch



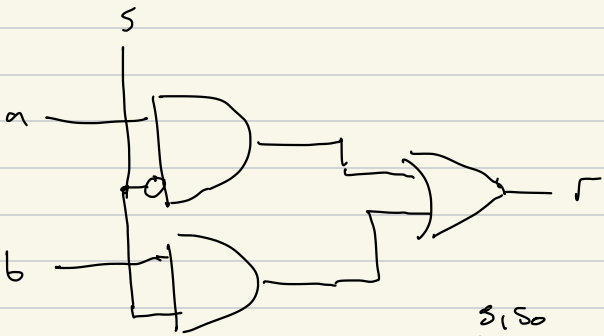
Clock

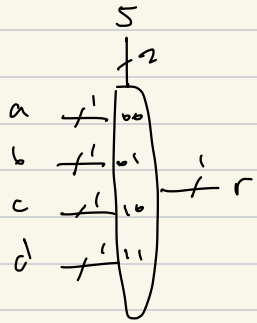
Multiplexor

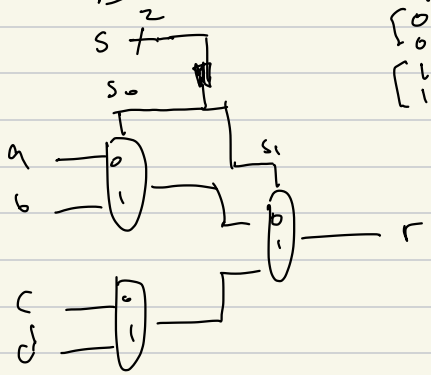


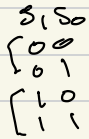


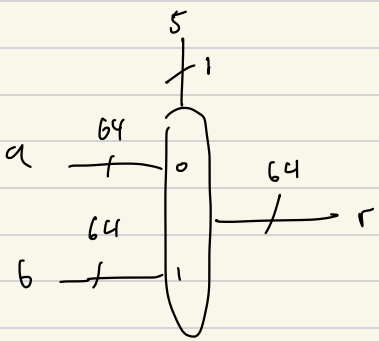
a	b	s	r
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1



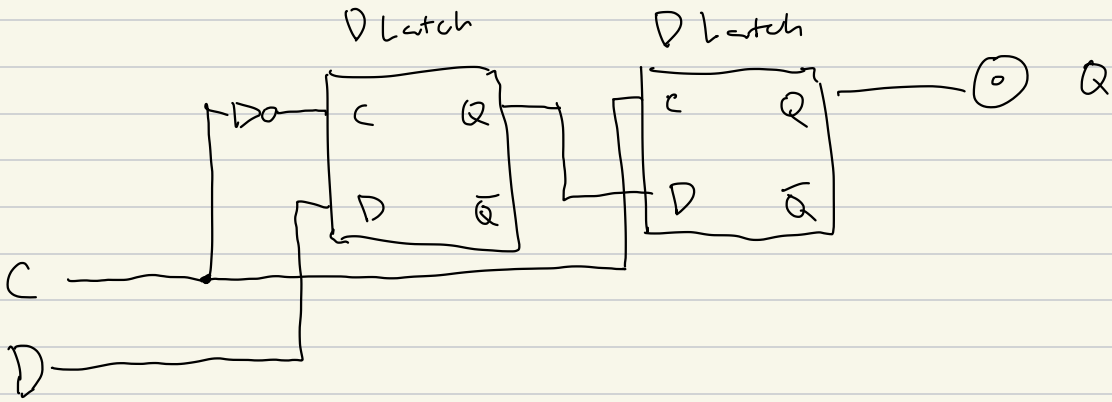




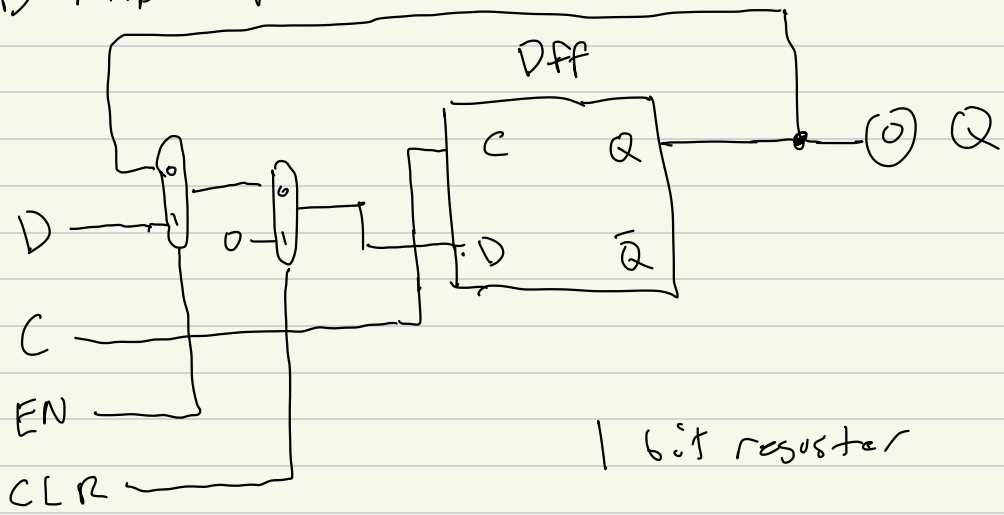




D Flip Flop

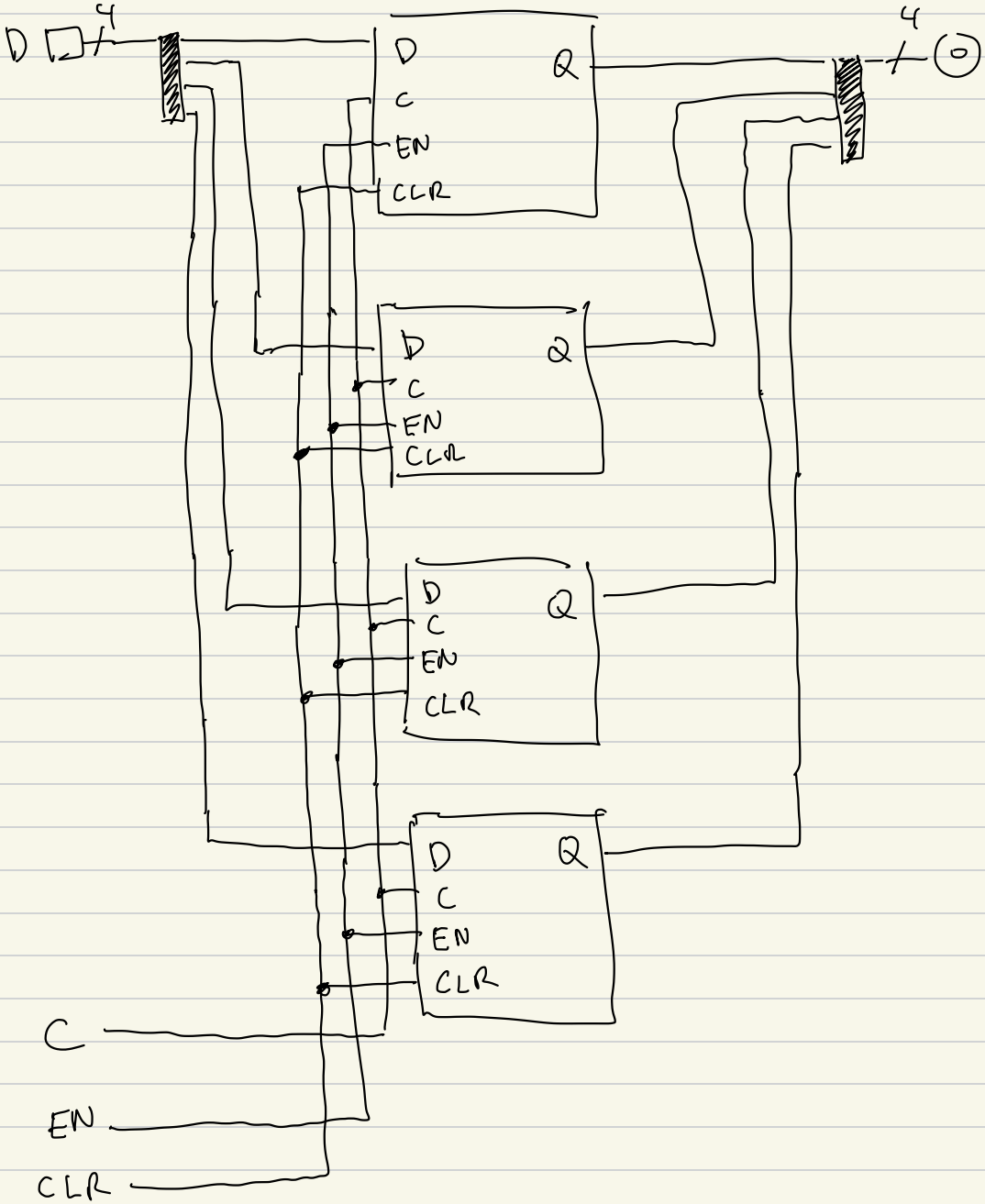


D Flip Flop with CLR an EN



1 bit resister

4-bit register



4-bit counter